PROGRAMME EDUCATIONAL OBJECTIVES (PEOs):

I. To enrich students to excel in research leading to cutting edge technology in VLSI design and embedded systems and creating competent, innovative, and productive professionals in this field.

II. To provide students with a solid foundation in digital and computer architecture principles leading to VLSI design.

III. To understand the various applications and employ embedded systems to find solutions to them with good scientific and engineering knowledge so as to comprehend, analyze, design, and create novel products and solutions for the real life problems.

IV. To provide students with an academic environment aware of excellence, leadership, ethical conduct, positive attitude, societal responsibilities and the lifelong learning needed for a successful professional career.

V. To inculcate entrepreneurial skills in starting industries applying embedded system technologies.

PROGRAMME OUTCOMES (POs):

On successful completion of the programme,

1. Graduates will be able to apply the knowledge of computing, mathematics, science and electronic engineering for designing VLSI circuits.

2. Graduates will have an ability to identify, formulate, investigate and solve the issues related to the design of VLSI and embedded systems.

3. Graduates will have an ability to design and conduct experiments, perform analysis and interpret the problems of VLSI design and embedded systems.

4. Graduates will be able to demonstrate the design of an embedded system, component or process as per needs and specifications.

5. Graduates will demonstrate an ability to visualize and work on laboratory and multidisciplinary tasks.

6. Graduates will have the skills to use modern engineering tools, softwares and equipments to analyze problems.

7. Graduates will demonstrate knowledge of professional and ethical responsibilities.

8. Graduate will be able to communicate effectively in both verbal and written form.

9. Graduate will show the understanding of the impact of engineering solutions on the society and also will be aware of contemporary issues.

10. Graduate will develop confidence in self education and ability for lifelong learning.
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ANNA UNIVERSITY, CHENNAI
UNIVERSITY DEPARTMENTS
M.E. VLSI DESIGN AND EMBEDDED SYSTEMS
REGULATIONS – 2015
CHOICE BASED CREDIT SYSTEM
CURRICULA AND SYLLABI
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### VI SEMESTER

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# Employability Enhancement Courses (EEC)

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OBJECTIVES:
- To encourage students to develop a working knowledge of the central ideas of linear algebra;
- To study and understand the concepts of probability and random variable of the various functions;
- To understand the notion of a Markov chain, and how simple ideas of conditional probability and matrices can be used to give a thorough and effective account of discrete-time Markov chains;
- To formulate and construct a mathematical model for a linear programming problem in real life situation;
- To introduce the Fourier Transform as an extension of Fourier techniques on periodic functions and to solve partial differential equations.

UNIT I  LINEAR ALGEBRA  12

UNIT II  ONE DIMENSIONAL RANDOM VARIABLES  12

UNIT III  RANDOM PROCESSES  12
Classification – Auto correlation - Cross correlation - Stationary random process – Markov process — Markov chain - Poisson process – Gaussian process.

UNIT IV  LINEAR PROGRAMMING  12

UNIT V  FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS  12

TOTAL :60 PERIODS

OUTCOMES:
On successful completion of this course, students will be able to
- Classify the random process.
- Formulate and develop a mathematical model for linear programming problem
- Apply the concept of fourier transform to real life situation

REFERENCES:
OBJECTIVES:
- To study and realize various building blocks of digital VLSI circuits in transistor level.
- To design the architectural choices and performance tradeoffs involved and to realize circuits in CMOS technology.
- To introduce the design knowledge about CMOS testing and its implementation strategies.

UNIT I MOS TRANSISTOR PRINCIPLES
MOS Technology and VLSI, Pass transistors, NMOS, CMOS Fabrication process and Electrical properties of CMOS circuits and Device modeling, Characteristics of CMOS inverter, Scaling principles and fundamental limits. Propagation Delays, CMOS inverter scaling, Stick diagram, Layout diagram, Layout rules, Elmore’s constant, Logical Effort.

UNIT II COMBINATIONAL LOGIC CIRCUITS
Static CMOS logic Design, Design techniques to improve the speed, power dissipation of CMOS logic, low power design techniques, Ratioed logic, Pass transistor Logic, Transmission gate logic, CPL, DCVSL, Dynamic CMOS logic, Domino logic, Dual Rail logic, NP CMOS logic and NOR array logic.

UNIT III SEQUENTIAL LOGIC CIRCUITS
Static and Dynamic Latches and Registers, Timing Issues, Pipelines, Clocking strategies, Memory Architectures, and Memory control circuits.

UNIT IV DESIGNING ARITHMETIC BUILDING BLOCKS & TESTING
Datapath circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area tradeoffs.

UNIT V CMOS TESTING AND IMPLEMENTATION STRATEGIES
Need for testing - Manufacturing test – Design for testability – Boundary scan, Full Custom and Semicustom Design, FPGA building block architectures, FPGA interconnects.

OUTCOMES:
After completion of this course:
- Ability to expand their knowledge in designing circuit level implementation to realize and test system based architectures, which include digital, memory, and mixed-signal subsystems.

REFERENCES:
OBJECTIVES:
- To learn about the designing of an embedded system for commercial applications.
- To learn the features, architecture and programming of PIC and ARM microcontrollers.
- To study the interfacing peripherals with microcontrollers.
- To learn about the communication protocols in a Microcomputer system.
- To learn about the fundamentals of real-time operating system in an embedded system.

UNIT I INTRODUCTION TO EMBEDDED SYSTEMS

UNIT II PIC MICROCONTROLLERS
PIC 16F877 MCU, Architecture, Features, Memory and memory map, I/O ports, Timers and CCP Devices, ADC, Interrupts, Instruction format, Addressing Modes, Instruction Set, Programming with MPLAB IDE.

UNIT III ARM BASED MICROCONTROLLERS
Introduction to 16 bit Processors, ARM Architecture, ARM cortex M3, 16 bit ARM Instruction set, Thumb Instruction set, Exception Handling in ARM, Porting Linux in ARM, Assembly and C programming.

UNIT IV INTERFACING I/O DEVICES AND COMMUNICATION PROTOCOLS
LED, liquid crystal display, Motor (DC, Servo, Stepper), Relays, Keypad, Keyboard, Touch screen, Sensors (thermocouple, force, displacement), SD card, Infrared connectivity, Serial communication protocols (UART, I2C, SPI, CAN, USB, LIN), Parallel communication protocols (PCI, ISA), Wireless communication networks (Bluetooth, Xbee, Wifi, GSM), Global positioning system receivers, Embedded Systems and the internet.

UNIT V MULTITASKING AND THE REAL-TIME OPERATING SYSTEM
The challenges of multitasking and real-time, Achieving multitasking with sequential programming, RTOS, Scheduling and the scheduler, Developing tasks, Data and resource protection- the semaphore, Examples using Salvo Real-time operating systems.

TOTAL: 45 PERIODS

OUTCOMES:
After completion of this course:
- Students will be able to interface peripherals with microcontrollers.
- Students will be able to design an embedded system in real time.
- Students will be able to use the communication protocols in application specific.

REFERENCES:
OBJECTIVES:
- The course will discuss the equivalent circuits and models of MOS circuits.
- To analyze bias circuits using CMOS current mirrors.
- To design and analyze the frequency response of multistage differential amplifiers.
- To discuss the stability and frequency compensation of feedback amplifiers.

UNIT I  SINGLE STAGE AMPLIFIERS  9
Review of MOS physics and equivalent circuits and models. Large and Small signal analysis CS, CG and source follower, miller effect, frequency response of CS, CG and source follower.

UNIT II  CURRENT MIRRORS  6
Current Sources, Basic Current Mirrors, Cascode stages for Current mirrors, Wilson Current Mirror, Large and small signal analysis of current mirrors.

UNIT III  MULTISTAGE DIFFERENTIAL AMPLIFIERS  12
Differential amplifier, Large and small signal analysis of the balanced differential amplifier, device mismatches in differential amplifier, small and large signal analysis of the differential pair with current mirror load, PSRR+, PSRR− and CMRR of differential amplifiers, small signal analysis of telescopic amplifier, two-stage amplifier and folded cascaded amplifier.

UNIT IV  FREQUENCY RESPONSE OF MULTISTAGE DIFFERENTIAL AMPLIFIERS  9
Dominant-Pole approximation, zero-value time constant analysis, - Frequency response of current mirror loaded, differential amplifier, short circuit time constants, frequency response of telescopic cascaded, folded cascode amplifier.

UNIT V  STABILITY AND FREQUENCY COMPENSATION OF FEEDBACK AMPLIFIERS  9
Properties and types of negative feedback circuits, feedback configurations, effect of loading in feedback networks, feedback circuit analysis using return ratio- modelling input and output port in feedback network, the relation between gain and bandwidth in feedback amplifiers, phase margin, frequency compensation, compensation of two stage MOS amplifiers.

TOTAL:45 PERIODS

OUTCOMES:
After completion of this course, students are expected to:
- Be able to analyze and design CMOS analog IC building blocks like MOS amplifiers, current mirrors and multistage differential amplifiers.

REFERENCES:
OBJECTIVES:
- To describe the various fault models and to understand the fundamentals of fault detection.
- To understand the difficulties of sequential circuit tests.
- To understand the basic principles of test vector generation and to describe the basic principles of testable circuit design.
- To understand the principles of built-in self test and boundary scan standard.
- To discuss the structured design for testability techniques for system-on-a-chip design and automatic test equipment.

UNIT I INTRODUCTION TO TESTING 9

UNIT II FAULT MODELLING AND SIMULATION 9

UNIT III ATPG FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

UNIT IV BUILT-IN SELF-TEST & BOUNDARY SCAN STANDARD 9
Ad-Hoc DFT Methods and Scan Design, Economic Case for BIST, Random Logic BIST, Memory BIST, Delay Fault BIST - Purpose of Standard, System Configuration with Boundary Scan, Boundary Scan Description Language.

UNIT V SYSTEM TEST AND CORE-BASED DESIGN 9

TOTAL:45 PERIODS

OUTCOMES:
After completion of this course, students are:
- Well equipped with the concepts of testable circuit designs and testability techniques for system-on-a-chip design and automatic test equipment.

REFERENCES:
5. Alfred Crouch, Design for test for digital IC & Embedded Core Systems, Prentice Hall, 2002
7. Alfred L. Crouch, Design-for-Test for Digital IC's and Embedded Core Systems, Prentice Hall PTR.
OBJECTIVES:
- To understand the various analog and digital circuits and their simulation using Cadence tool.
- To learn the advanced concepts of modern VLSI circuit and system design
- To design common sequential functions: flip-flops, registers, latches, and state-machines.
- To understand placement, routing, and verify timing of a standard cell design.

DIGITAL DESIGN LAB WITH CADENCE:
1. HDL based design entry and simulation of Parameterizable cores of Counters, Shift registers, State machines, 8-bit Parallel adders and 8-Bit multipliers.
2. HDL based design entry and simulation of Parameterizable cores on the simple Distributed Arithmetic system.
3. HDL based design entry and simulation of Parameterizable cores on memory design and 4 – bit ALU.
4. Synthesis, P&R and post P&R simulation, Critical paths and static timing analysis results to be identified.

ANALOG IC DESIGN WITH CADENCE VIRTUOSO:
Circuit simulation, Layout generation, parasitic extraction, Synthesis and Standard cell based design of the circuits. Identification of critical paths, power consumption. P&R, power and clock routing, post P&R simulation and Static timing analysis of:
1. Design of CMOS Inverter - Circuit Simulation, transfer characteristic curve, transient analysis, Layout design.

TOTAL : 60 PERIODS

OUTCOMES:
After the completion of this lab, Students should be able:
- To create the hierarchical decomposition of sequential designs.
- To perform synthesis and analysis of combinational and sequential designs.

OBJECTIVES:
- To understand the basics of embedded system, architecture of PIC microcontroller and ARM processor.
- To understand the RTOS concepts like scheduling and memory management related to the embedded system.
- To learn the protocols of embedded wireless application.
- To understand concepts involved in the design of hardware and software components for an embedded system.

UNIT I
INTRODUCTION
UNIT II  EMBEDDED/REAL TIME OPERATING SYSTEM  9

UNIT III  CONNECTIVITY  9

UNIT IV  REAL TIME UML  6

UNIT V  SOFTWARE DEVELOPMENT AND CASE STUDY  9

TOTAL: 45 PERIODS

OUTCOMES:
• To be able to make a choice a suitable embedded processor for a given application.
• To be able to design the hardware and software for the embedded system.
• To be able to design and develop the real time kernel/operating system functions, task control block structure and analyze different task states.
• To be able to implement different types of inter task communication and synchronization techniques.

REFERENCES:

VE7202  VLSI ARCHITECTURES FOR SYSTEM DESIGN  L T P C
3 0 0 3

OBJECTIVES:
• This course will introduce the features, programming and applications of programmable logic devices.
• Provide VLSI system design experience using FSM.
• Discuss the various implementation strategies with FPGA.

UNIT I  PROGRAMMABLE LOGIC  9
ROM, PLA, PAL, PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series, CPLD, Cypres FLASH 370 Device Technology, Lattice LSI’s Architectures – 3000 Series – Speed Performance and in system programmability.
UNIT II  FPGAS: FIELD PROGRAMMABLE GATE ARRAYS  
Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs, Case studies – Xilinx Virtex-6, Spartan-6 FPGAs, ALTERA’s FLEX 8000/10000 FPGAs, NIOS II Embedded Processor, ACTEL’s IGLOO series, ProASIC3 series FPGAs.

UNIT III  FINITE STATE MACHINES (FSM)  

UNIT IV  FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN  
Architectures centered around non-registered PLDs. State machine design centered around shift registers. One – Hot design method. Use of ASMs in One – Hot design. K Application of One – Hot method. System level design – controller, data path and functional partition.

UNIT V  IMPLEMENTING APPLICATIONS WITH FPGAS  

TOTAL: 45 PERIODS

OUTCOMES:  
After the completion of this course, the students are to:

- Be able to make the system level designs using FSM and analyze the performance with FPGA.

REFERENCES:  
5. Scott Hauck and Andre DeHon Reconfigurable Computing The Theory and Practice of FPGA based Computation Morgan Kaufmann Publishers

VE7201  HARDWARE SOFTWARE CO DESIGN OF EMBEDDED SYSTEM  

OBJECTIVES:  
- To introduce the key concepts of hardware/software communication to make trade-offs between the flexibility and the performance of a digital system.
- To learn the concept of integration of custom hardware components with software.
- Students will gain design and implementation experience with case studies.

UNIT I  NATURE OF HARDWARE AND SOFTWARE  
Hardware, Software, Definition of Hardware/Software Co-Design – Driving factors Platform design space – Application mapping – Dualism of Hardware design and software design – Concurrency and parallelism, Data flow modeling and Transformation – Data Flow Graph – Tokens, actors and queues, Firing rates, firing rules and Schedules – Synchronous data flow graph – control flow modeling – Adding time and resources – Trandformations.
UNIT II DATA FLOW IMPLEMENTATION IN SOFTWARE AND HARDWARE 9

UNIT III DESIGN SPACE OF CUSTOM ARCHITECTURES 9
Finite state machines with datapath – FSM design example, Limitations – Microprogrammed Architecture – Microprogrammed control, microinstruction encoding, Microprogrammed data path, microprogrammed machine – General purpose Embedded Core – RISC pipeline, Program organization – SoC interfaces for custom hardware – Design Principles in SoC Architecture

UNIT IV HARDWARE/ SOFTWARE INTERFACES 9
Principles of Hardware/software communication – synchronization schemes, communication constrained versus Computation constrained, Tight and Loose coupling - On-chip buses – Memory mapped interfaces – coprocessor interfaces – custom instruction interfaces – Coprocessor hardware interface – Data and control design, programmer’s model.

UNIT V CASE STUDIES 9

TOTAL:45 PERIODS

OUTCOMES:
On completion of the course, a student should be able:
- To analyze and apply design methodologies.
- To appreciate the fundamental building blocks of the using hardware and software co-design and related implementation and testing environments and techniques and their interrelationships.
- To be familiar with modern hardware/software tools for building prototypes and to be able to demonstrate practical competence in these areas

REFERENCES:

VL7252 LOW POWER VLSI DESIGN L T P C
3 0 0 3

OBJECTIVES:
- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation and design memory circuits with low power dissipation.

UNIT I POWER DISSIPATION IN CMOS 9
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.
UNIT II  POWER OPTIMIZATION  9
Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT III  DESIGN OF LOW POWER CMOS CIRCUITS  9
Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques – Special techniques.

UNIT IV  POWER ESTIMATION  9
Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V  SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER  9
Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

OUTCOMES:
• The student will get to know the basics and advanced techniques in low power design which is a hot topic in today’s market where the power plays major role.
• The reduction in power dissipation by an IC earns a lot including reduction in size, cost and etc.

REFERENCES:

VE7211  EMBEDDED SYSTEMS LAB  L  T  P  C
0  0  4  2

OBJECTIVES:
• Students have knowledge about the basic functions of embedded systems.
• Students have knowledge in programming skills.

EXPERIMENTS:
ARM/ PIC Microcontroller based Experiments with MPLAB IDE from Microchip/ μVision IDE for ARM programming from Keil:

1. Interfacing basic digital input output devices.
2. Interfacing a character LCD.
3. Interfacing A/D and D/A converter.
4. Interfacing Capture/Compare/PWM module.
5. DC motor control.
6. Multiplexing seven segment LED displays.
7. Interfacing Stepper motor and temperature sensor.
8. Traffic light controller using Keil real time Kernel.

TOTAL : 60 PERIODS
OUTCOMES:
- An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, and sustainability.

VE7301 SoC DESIGN FOR EMBEDDED SYSTEM

OBJECTIVES:
- To introduce architecture and design concepts underlying system on chips.
- Students can gain knowledge of designing SoCs.
- To impart knowledge about the hardware-software design of a modest complexity chip all the way from specifications, modeling, synthesis and physical design.

UNIT I SYSTEM ARCHITECTURE: OVERVIEW
Components of the system – Processor architectures – Memory and addressing – system level interconnection – SoC design requirements and specifications – design integration – design complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability.

UNIT II PROCESSOR SELECTION FOR SOC

UNIT III MEMORY DESIGN

UNIT IV INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION

UNIT V FPGA BASED EMBEDDED PROCESSOR

TOTAL: 45 PERIODS

OUTCOMES:
Upon successful completion of the program the students shall
- Explain all important components of a System-on-Chip and an embedded system, i.e. digital hardware and embedded software;
- Outline the major design flows for digital hardware and embedded software;
- Discuss the major architectures and trade-offs concerning performance, cost and power consumption of single chip and embedded systems;
REFERENCES:

NE7072        ASIC DESIGN     L T P C
                3 0 0 3

OBJECTIVES:
- To study the basic concepts of digital CMOS Application Specific Integrated Circuit (ASIC) systems design and library cell design.
- To know the architectural details of programmable ASICs.
- To present the ASIC physical design flow, including logic synthesis, floor-planning, placement and routing.
- To know back-end physical design flow steps through VLSI CAD tools.

UNIT I       INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN   9
Types of ASICS - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors – Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II     PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS   9
Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III     PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY   9

UNIT IV      LOGIC SYNTHESIS, SIMULATION AND TESTING   9
Verilog and logic synthesis - VHDL and logic synthesis - types of simulation - boundary scan test - fault simulation - automatic test pattern generation.

UNIT V      ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING   9
System partitioning - partitioning methods - floor planning - placement - physical design flow – Routing - global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL:45 PERIODS

OUTCOMES:
Upon completion of this course, the students will:
- Be able to design the ASIC implementation using programmable ASIC devices.
- Be able to comprehend the different issues related to the development of ASIC designs including logic synthesis, floor-planning, placement and routing, tools and future trends.

REFERENCES:
VL7073 VLSI SIGNAL PROCESSING L T P C 3 0 0 3

OBJECTIVES:
- This course will introduce approaches and methodologies for VLSI design of signal processing.
- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9
Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9
Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

TOTAL: 45 PERIODS

OUTCOME:
- Students will be able to modify the existing or new DSP architectures suitable for VLSI

REFERENCES:
VE7016 RF IC DESIGN L T P C 3 0 0 3

OBJECTIVES:
- To understand the fundamentals of RF integrated circuits operating at microwave frequencies.
- To learn RFIC design techniques, including system architecture, key building blocks design methodologies in CMOS technology.

UNIT I COMPONENTS FOR RF IC
MOSFET Physics: Long channel and Short channel approximation, Noise: Two port Noise theory, MOS capacitor, Spiral Inductors, Model for on chip inductors, Bond wire inductors, Monolithic transformer realization, Interconnects.

UNIT II CIRCUIT DESIGN FOR LOW NOISE AMPLIFIERS
Methods of Open circuit and Short circuit time constants, Bandwidth enhancers, Tuned amplifier, Neutralisation, cascaded amplifiers, CMOS amplifiers, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III POWER AMPLIFIER DESIGN
Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, Class A, AB, B, C, D, E and F amplifiers, Linearization Techniques, RF power amplifier design example.

UNIT IV PLL AND FREQUENCY SYNTHESIZERS
Linearized PLL Model, Noise properties, Phase detectors, Loop filters and Charge pumps, PLL Design examples. Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

UNIT V SYSTEM ARCHITECTURE
Receiver architecture: Noise figure, Linearity in cascaded systems, Single and Dual conversion receivers, Image reject receivers, Direct conversion. Transmitter architectures, Detailed Chip design example: WLAN Transceiver architecture.

TOTAL: 45 PERIODS

OUTCOMES:
- Ability to analyze the high frequency effects on basic circuit components.
- Ability to design RF LNAs and receivers.
- Ability to design RF power amplifiers.
- Ability to design PLL and frequency synthesizers

REFERENCES:

VE7011 MEMS AND MICROSYSTEMS L T P C 3 0 0 3

OBJECTIVES:
- To understand the fundamentals of MEMS and Microsystems.
- To learn MEMS accelerometers and actuators design techniques, including interfacing and packaging techniques.
UNIT I  INTRODUCTION TO MEMS  9
MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II  MICROMECHANICS  9
Elasticity, Stress, strain and material properties, Bending of thin films, Spring configurations, torsion deflection, Mechanical vibration, Resonance, Thermomechanics - actuators, force and response time, Fracture and thin film mechanics.

UNIT III  MICROACTUATORS  9
Electrostatics: basic theory, electrostatic instability. Surface tension, Gap and finger pull up, Electrostatic actuators, comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators, bistable actuators.

UNIT IV  INTERFACING AND PACKAGING  9
Electronic Interfaces, Feedback systems, Noise, Packaging: Dicing-Wafer level Packaging-Wafer bonding-Connections between layers-self assembly-higher level of packaging.

UNIT V  CASE STUDIES  9
Optical MEMS, RF MEMS- System design basics, Case studies: Capacitive accelerometer, Peizo electric pressure sensor, MEMS scanners, Capacitive RF MEMS switch, performance issues.

TOTAL: 45 PERIODS

OUTCOMES:
Upon completion of the course, students will have:
- An ability to analyze the working of MEMS and Microsystems components.
- An ability to design the MEMS accelerometer and to design Electrostatic actuators.
- An ability to analyze the working of RF and Optical MEMS.

REFERENCES:

VE7013  NANO ELECTRONICS  L T P C
3 0 0 3

OBJECTIVES:
- To discuss the fundamentals of nanoelectronics and nanocomputer architectures.
- To impart knowledge about the concepts of nano fabrication, nanostructures and nano phase materials.
- To describe the principle and the operation of nanoelectronic devices.
- To explain the principle and application of spintronic devices.

UNIT I  INTRODUCTION  9
Recent past, the present and its challenges, Future, Overview of basic Nano electronics.

UNIT II  NANO ELECTRONICS & NANOCOMPUTER ARCHITECTURES  9
UNIT III  NANO ELECTRONIC ARCHITECTURES  9

UNIT IV  SPINTRONICS  9
Introduction, Overview, History & Background, Generation of Spin Polarization Theories of spin Injection, spin relaxation and spin dephasing, Spintronic devices and applications, spin filters, spin diodes, spin transistors. Memory Devices And Sensors.

UNIT V  MEMORY DEVICES AND SENSORS  9

TOTAL: 45 PERIODS

OUTCOMES:
- Ability to discuss the fundamentals of nanoelectronic architectures and its components.
- Ability to explain the principles of nanoelectronics, nanodevices, spintronics and molecular electronics.

REFERENCES:

VE7018  VLSI FOR WIRELESS COMMUNICATION  L T P C
3 0 0 3

OBJECTIVES:
- To cover the design of VLSI circuits used in modern wireless transceivers.
- To illustrate the design trade-offs in the transceivers with practical, real life circuit examples, with low power as an important design objective.
- To discuss the architectures of wireless transceivers at the transistor level, using submicron CMOS.
- To discuss the circuits such as low noise amplifiers, mixers, power amplifiers, oscillators, phase locked loops and A/D and D/A converters.

UNIT I  COMMUNICATION CONCEPTS  9

UNIT II  TRANSMITTER AND RECEIVER ARCHITECTURES:  9
Transmitter backend, Quadrature LO generator, Receiver Front End; Filter Design, Rest of Receiver Front End, Derivation of NF, IIP3 of Receiver Front End - Wideband LNA Design, Narrow Band LNA; Impedance Matching, Core Amplifier.

UNIT III  ACTIVE AND PASSIVE MIXER  9
Active Mixer: Balancing, Qualitative Description of the Gilbert Mixer, Distortion, Low Frequency Case: Analysis of Gilbert Mixer, Distortion, High Frequency Case, Noise

**UNIT IV ANALOG-TO-DIGITAL CONVERTERS**

**UNIT V FREQUENCY SYNTHESIZER:**
PLL based frequency synthesizer, Phase detector/Charge pump, VCO, Dividers, Ring oscillators, Loop filter – General description, Design approaches.

**OUTCOMES:**
- Ability to design wireless transceivers using low noise amplifiers, mixers, power amplifiers, oscillators, phase locked loops, A/D and D/A converters and frequency synthesizers.

**REFERENCES:**

**VE7015 PARALLEL AND RECONFIGURABLE ARCHITECTURES**

**OBJECTIVES:**
- The student shall develop an overview and deeper insight into the research and development that is underway to meet future needs of flexible processor solution, for energy efficient reconfigurable architectures with high computing performance.

**UNIT I INTRODUCTION**
Reconfigurable Computing Systems (RCS) – Evolution of reconfigurable systems – Characteristics of RCS - Advantages and issues, Fundamental concepts & Design steps, Domain specific processors, Application specific processors, Classification of reconfigurable architecture - fine, coarse grain & hybrid architectures

**UNIT II PARALLEL AND ADVANCED PROCESSORS**
Classification of parallel computers, Multiprocessors and multicomputer, SIMD Processing Architectures, CISC & RISC Processors, VLIW Architectures

**UNIT III RECONFIGURABLE ARCHITECTURES**
FPGA Technology and Architectures – LUT devices and mapping (Look-up Table) ALU design – Placement and partitioning algorithms – Routing algorithms, Spatial Computing Architectures – Systolic Architectures and Algorithms Systolic Structures

**UNIT IV RECONFIGURATION MANAGEMENT**
Reconfiguration, Configuration Architectures, Managing the Reconfiguration Process, Reducing Configuration Transfer Time
UNIT V CASE STUDIES OF FPGA APPLICATIONS


TOTAL: 45 PERIODS

OUTCOMES:
Upon successful completion of the course, the student should be able to:

- Analyze the different architecture principles relevant in parallel and reconfigurable systems.
- Compare the tradeoffs that are necessary to meet the area, power and timing criteria of these systems.
- In depth analysis of current research projects to get broader context and assess its significance.
- Describe and relate new architectures and applications in relations to the previously existing solutions.

REFERENCES:

VE7001 ADVANCED CMOS ANALOG IC DESIGN

OBJECTIVES:
- To provide the fundamental concepts of noise in IC, OTA design, switched-capacitor circuits and data conversion circuits.

UNIT I NOISE IN INTEGRATED CIRCUITS
Statistical Characteristics of Noise, Sources of noise, noise models of IC components, Circuit noise calculations, equivalent input noise generators, effect of feedback on noise performance, noise in CS, CE, CG and cascode amplifiers, noise in differential pair, noise bandwidth.

UNIT II OTA DESIGN CONSIDERATION
Step response, Slewing, OTA variations, CMFB implementation, Input resistance, Output resistance, Output Voltage swing, CMRR, PSRR of two-stage telescopic amplifiers.

UNIT III BANDGAP REFERENCE CIRCUIT AND SWITCHED CAPACITOR CIRCUITS
UNIT IV PERFORMANCE METRICS OF DATA CONVERTERS & NYQUIST RATE D/A CONVERTERS

Ideal Sampling, Reconstruction, Quantization, Static performance metrics, Dynamic performance metrics, Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs.

UNIT V ANALOG TO DIGITAL CONVERTERS

Single stage amplifier as comparator, resistor-based latched comparators. offset cancellation, Flash ADC, Successive approximation ADC, Pipelined ADC, Time Interleaved ADC.

TOTAL: 45 PERIODS

OUTCOMES:
At the completion of the subject, students should:

- Be able to grasp the fundamental concept of noise in IC.
- Be able to study and analyze switched-capacitor circuits and the issue of non-linearity and mismatch in the circuits.
- Be able to analyze data conversion circuits such as DAC and ADC and their design techniques.

REFERENCES:

NE7074 COMPUTATIONAL INTELLIGENCE

OBJECTIVES:
- To provide the basic concepts in computational intelligence.
- To give an exposure to neural network learning techniques and architectures.
- To provide a good understanding of fuzzy concepts and models.
- To provide an exposure to different optimization techniques.

UNIT I INTRODUCTION TO COMPUTATIONAL INTELLIGENCE

Evolution of Computing - Constituents - From Conventional AI to Computational Intelligence - Machine Learning Basics

UNIT II NEURAL NETWORKS

Biological Neurons Networks – Artificial Neural Networks - Supervised -.unsupervised learning - Reinforcement Learning – Activation functions - Perceptrons - Back Propagation networks – Radial Basis Function Networks - Adaptive Resonance architectures - Advances in Neural networks –SVM

UNIT III FUZZY LOGIC

UNIT IV NEURO-FUZZY MODELING

UNIT V OPTIMIZATION ALGORITHMS

TOTAL = 45 PERIODS

OUTCOMES:
- To be able to design systems based on neural network architectures.
- To implement fuzzy models and work on the fuzzy tool box.
- To design a suitable optimization algorithm for a given application

REFERENCES:

AP7073 DESIGN AND ANALYSIS OF COMPUTER ALGORITHMS

OBJECTIVES:
- To discuss the algorithmic complexity parameters and the basic algorithmic design techniques.
- To discuss the graph algorithms, algorithms for NP Completeness Approximation Algorithms and NP Hard Problems.

UNIT I INTRODUCTION
Polynomial and Exponential algorithms, big "oh" and small "oh" notation, exact algorithms and heuristics, direct / indirect / deterministic algorithms, static and dynamic complexity, stepwise refinement.

UNIT II DESIGN TECHNIQUES
Subgoals method, working backwards, work tracking, branch and bound algorithms for traveling salesman problem and knapsack problem, hill climbing techniques, divide and conquer method, dynamic programming, greedy methods.

UNIT III SEARCHING AND SORTING
Sequential search, binary search, block search, Fibonacci search, bubble sort, bucket sorting, quick sort, heap sort, average case and worst case behavior
UNIT IV  GRAPH ALGORITHMS  
Minimum spanning, tree, shortest path algorithms, R-connected graphs, Even's and Kleitman's algorithms, max-flow min cut theorem, Steiglitz's link deficit algorithm.

UNIT V  SELECTED TOPICS  

TOTAL: 45 PERIODS

OUTCOMES:
- Will be able to apply the suitable algorithm according to the given optimization problem.
- Ability to modify the algorithms to refine the complexity parameters.

REFERENCES:

VE7007  DISTRIBUTED EMBEDDED COMPUTING  
L T P C  
3 0 0 3

OBJECTIVES:
- To expose the students to the fundamentals of Network communication technologies.
- To teach the fundamentals of Internet
- To study on Java based Networking
- To introduce network routing Agents
- To study the basis for network on-chip technologies

UNIT I  THE HARDWARE INFRASTRUCTURE  

UNIT II  INTERNET CONCEPTS  
Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

UNIT III  DISTRIBUTED COMPUTING USING JAVA  

UNIT IV  EMBEDDED AGENT  

UNIT V  EMBEDDED COMPUTING ARCHITECTURE  

TOTAL : 45 PERIODS
OUTCOMES:
At the completion of the course, students will be able to:

- Explain the fundamentals of Network communication technologies, internet, and Java based networking.
- Analyze the analog/digital co-design of distributed embedded computing architecture.

REFERENCES:

VE7017 ROBOTICS

OBJECTIVES:

- To learn about the dynamics of robotic controls
- To learn about the navigation mechanisms
- To learn about the hardware and software tools required for building robotic systems

UNIT I INTRODUCTORY ROBOTICS
Introduction, Rigid Transformation, Robot anatomy, Kinematics, Inverse Kinematics, Jacobians, Trajectory Following, Statics and Dynamics.

UNIT II ARTIFICIAL LIFE AND ARTIFICIAL INTELLIGENCE

UNIT III HARDWARE TOOLS
Microcontroller, Photovoltaic Cells, Fuel Cells, Batteries.
Movement and Drive Systems- Air muscles, Nitinol wire, Solenoids, Rotary solenoids, Stepper motors, Servo Motors and DC motors.
Sensors-Signal conditioning, Light sensors, Machine vision, Body sense, Direction-magnetic fields, Speech recognition, Sound and ultrasonics, Touch and Pressure, Piezoelectric material, Switches, Bend sensors, Pressure sensor, Smell, Humidity, Testing sensor.

UNIT IV BASIC NAVIGATION

UNIT V DESIGN OF ROBOTS
Telepresence robot, Mobile platforms, Walker Robots, Solar-ball Robot, Underwater bots, Aerobots, Robotic arm and IBM PC interface and speech control, Android hand.

TOTAL: 45 PERIODS

OUTCOMES:
Students will be able to

- Build a miniature robotic system
- Explain navigation mechanisms involved in building a robotic system
REFERENCES:

VE7002 ADVANCED EMBEDDED SYSTEM DESIGN

OBJECTIVES
- To teach the fundamentals on design attributes of functional units of embedded systems.
- To discuss about Hardware, software partitioning in system design
- To introduce architectural features of 32 bit ARM microcontroller.
- To discuss strategies for embedded firmware design and development.
- To develop an integrated development environment in embedded system

UNIT I TYPICAL EMBEDDED SYSTEM

UNIT II EMBEDDED HARDWARE DESIGN AND DEVELOPMENT
EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus , port, junction, creating part numbers, Design Rules check, Bill of materials, Netlist creation , PCB Layout Design – Building blocks, Component placement.

UNIT III ARM -32 BIT MICROCONTROLLER FAMILY

UNIT IV EMBEDDED FIRMWARE DESIGN AND DEVELOPMENT
Embedded Firmware Design Approaches, Embedded Firmware Development Languages, Real-Time Operating System (RTOS) based Embedded System Design: Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS

UNIT V EMBEDDED SYSTEM DEVELOPMENT ENVIRONMENT
The Integrated Development Environment (IDE), Types of Files Generated on Cross compilation, Disassembler/ELDompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

TOTAL: 45 PERIODS

OUTCOMES:
- Ability to discuss the concepts of typical embedded systems.
- Ability to develop an integrated development environment of hardware/software codesign of embedded system.
REFERENCES:

NE7071        ADAPTIVE SIGNAL PROCESSING        L T P C
                          3 0 0 3

OBJECTIVES:
• To provide an in-depth coverage of the adaptive filter theory.
• To provide the mathematical framework for the understanding of adaptive statistical signal processing.
• To know the basic tools of vector spaces and discrete-time stochastic process.
• To understand the various issues involved in adaptive filtering.
• Various types of adaptive filters will be introduced and their properties will be studied, specifically convergence, tracking, robustness and computational complexity.
• Learn to apply adaptive filter theory using prescribed case studies.

UNIT I        STOCHASTIC PROCESSES AND SPECTRUM ESTIMATION
9

UNIT II        WIENER FILTERS
9

UNIT III        GRADIENT-BASED ADAPTIVE FILTERS
9

UNIT IV        KALMAN FILTERS & TRACKING
9

UNIT V        APPLICATIONS
9

TOTAL: 45 PERIODS

OUTCOMES:
• To be able to solve the problems related to optimal design, convergence, and recursiveness.
• To carry out time/frequency domain implementations of adaptive filters.
• To be able to apply the concepts of stochastic processes to adaptive filters.
• To be able to design adaptive filter algorithms.
• To be able to apply adaptive filter theory to applications such as echo cancelation, noise cancellation and channel equalization.
REFERENCES:

VE7014 NETWORK ON CHIP DESIGN

OBJECTIVES:
- To impart knowledge in the concept of a peer to peer interconnection network, shared bus based design, and network on chip (NoC) based architectures.
- To address the issues of scalability of onchip connectivity and inter processor communication.

UNIT I INTRODUCTION TO INTERCONNECTION NETWORKS

UNIT II TYPES OF NETWORKS
Butterfly Networks, Torus Networks Mesh Networks, Non-blocking networks, Non-interfacing networks, Crossbar networks Clos Networks, Bene´s Networks, Sorting Networks

UNIT III ROUTING & FLOW CONTROL

UNIT IV QUALITY OF SERVICE & ROUTER
Guaranteed services, Best-Effort services, Router Datapath Components, Input Buffer organization, Switches, Output Organization, Arbitration, waveform allocator, Processor-Network Interface, Shared-Memory Interface.

UNIT V PERFORMANCE ANALYSIS

TOTAL: 45 PERIODS

OUTCOMES:
At the completion of this subject, students should be able to:
- Design and analyze NOC architectures with interconnection networks, routing, shared memory interface, Processor-Network Interface.

REFERENCES:
OBJECTIVES:
- To understand the basics of embedded C programming and its compilers and simulators.
- Apply to C programming in embedded systems.

UNIT I BASICS OF EMBEDDED C
System programming Vs Application Programming-General rules in C, Comments, White Spaces, Modules, Data type, Procedures, Variables, Expression and Statements, Structures and Union, Data structures, Program Description Language.

UNIT II PROGRAMMING
Adding Structure to the Code Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Examples.

UNIT III COMPLIERS AND SIMULATORS
Introduction to MikroC compiler and debugger, Functions and Inbuilt libraries in MikroC, Creating new libraries, Development Tools, Introduction to simulators such as Proteus and Real PIC.

UNIT IV EMBEDDED MEMORY
Mixing Assembly and C, Memory Alignment with Structures, Memory management in C, Memory-map of Applications.

UNIT V CASE STUDIES
Chasing LEDs, LED Dice, Seven Segment LED Counter, Two-Digit Multiplexed Seven Segment LED Counter with Timer Interrupt, Real Time Clock, Digital Voltmeter with LCD, Calculator with Keypad and LCD, Serial Communication Based Calculator, Multitasking and Real-Time Operating Systems.

OUTCOMES:
- This subject enables our students to create, develop, apply, and disseminate the programming knowledge within the embedded systems development environment.

REFERENCES:
UNIT I  LOGIC SYNTHESIS & VERIFICATION:  6
Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

UNIT II  PARTITIONING:  9
Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

UNIT III  PLACEMENT, FLOOR PLANNING & PIN ASSIGNMENT:  9
Problem formulation, simulation based placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

UNIT IV  GLOBAL ROUTING:  12
Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches Detailed Routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization.

UNIT V  COMPACTION:  9
Problem formulation, one-dimensional compaction, two dimensions based compaction, hierarchical compaction.

TOTAL: 45 PERIODS

OUTCOMES:
Ability to analyze the algorithms needed for synthesis, partitioning, placement, floor planning, routing in VLSI design automation

REFERENCES:

VE7008  EMBEDDED AUTOMOTIVE SYSTEMS  L T P C  3 0 0 3

OBJECTIVES
- To teach the Fundamentals of Electronic Components related to automotive applications.
- To discuss on Automotive Sensors, Actuators and Instrumentations
- To teach the Control Mechanisms in an Automotive System
- To discuss on Telematics and Diagnostic methods

UNIT I  SYSTEMS APPROACH TO CONTROL AND INSTRUMENTATION  9
UNIT II      FUNDAMENTALS OF ELECTRONICS, MICROCOMPUTER INSTRUMENTATION AND CONTROL

Semiconductor Devices, Transistors, ICs, Operational Amplifiers, Use of Feedback in Op Amps, Phase-Locked Loop, Digital Circuits, Logic Circuits (Combination and Sequential Circuits), Timers and Counters, Microcomputer fundamentals, Tasks and Operations, CPU Registers, Reading Instructions, Programming Languages, Microcomputer Hardware, Microcomputer Applications in Automotive Systems, Instrumentation Applications of Microcomputers, Microcomputers in Control Systems.

UNIT III   SENSORS, ACTUATORS AND ELECTRONIC ENGINE CONTROL


UNIT IV   MOTION AND DIGITAL POWERTRAIN CONTROL SYSTEM


UNIT V    AUTOMOTIVE INSTRUMENTATION, TELEMATICS AND ITS DIAGNOSTICS


TOTAL : 45 PERIODS

OUTCOMES:
At the successful completion of this course, students will be able to:
- Discuss embedded controls and mechanisms involved in an automotive systems

REFERENCES:

VE7004   COMPUTER AIDED DESIGN FOR VLSI CIRCUITS

OBJECTIVES:
- To discuss the Algorithmic Graph Theory and computational complexity optimization.
- To discuss the concepts of layout design rules and floor planning.
- To simulate and synthesis different hardware models.
UNIT I  VLSI DESIGN METHODOLOGIES  9

UNIT II  DESIGN RULES  9

UNIT III  FLOOR PLANNING  9
Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV  SIMULATION  9
Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V  MODELLING AND SYNTHESIS  9
High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.  

TOTAL : 45 PERIODS

OUTCOMES:
At the completion of this subject,
• Students will be able to implement, simulate and synthesis the computer aided design of VLSI systems.

REFERENCES:

VE7005  DESIGN OF EMBEDDED CONTROL SYSTEM  L T P C
3 0 0 3

OBJECTIVES:
• To expose the students to the fundamentals of Embedded System Blocks
• To teach the fundamental RTOS.
• To study on interfacing for processor communication
• To compare types and Functionalities in commercial software tools
• To discuss the Applications development using interfacing

UNIT I  EMBEDDED SYSTEM ORGANIZATION  9
Embedded computing, Characteristics of embedded computing applications, Embedded system design challenges, Build process of Realtime Embedded system, Selection of processor, Memory, I/O devices, Rs-485, MODEM, Bus Communication system using I2C, CAN, USB buses, 8 bit – ISA, EISA bus.

UNIT II  REAL-TIME OPERATING SYSTEM  9
Introduction to RTOS, RTOS- Inter Process communication, Interrupt driven Input and Output, Nonmaskable interrupt, Software interrupt, Thread – Single, Multithread concept, Multitasking Semaphores.
UNIT III  INTERFACE WITH COMMUNICATION PROTOCOL  9
Design methodologies and tools – Design flows – Designing hardware and software Interface, System Integration; SPI, High speed data acquisition and interface, SPI read/write protocol, RTC interfacing and programming.

UNIT IV  DESIGN OF SOFTWARE FOR EMBEDDED CONTROL  9

UNIT V  CASE STUDIES WITH EMBEDDED CONTROLLER  9
Programmable interface with A/D & D/A interface, Digital voltmeter, Control- Robot system, PWM motor speed controller, Serial communication interface.

TOTAL : 45 PERIODS

OUTCOMES:
• Students will be able to realize a real time embedded system.

REFERENCES:

VE7012  MULTICORE ARCHITECTURES AND PROGRAMMING  L T P C
3 0 0 3
OBJECTIVES:
• To discuss the principles of different multiprocessors with their performance issues.
• To discuss the fundamentals of various programming concepts used in multicore architectures.

UNIT I  INTRODUCTION TO MULTIPROCESSORS AND SCALABILITY ISSUES  9

UNIT II  PARALLEL PROGRAMMING  9

UNIT III  OPENMP PROGRAMMING  9
UNIT IV  MPI PROGRAMMING
MPI Model – collective communication – data decomposition – communicators and topologies – point-to-point communication – MPI Library.

UNIT V MULTICORE ARCHITECTURES FOR EMBEDDED SYSTEMS
Architectural Considerations, Interconnection Networks, Software Optimizations.

TOTAL : 45 PERIODS

OUTCOMES:
- Students will be able to explain the principle and operation of multicore architectures and their programming.
- Students will be able to design a multicore architecture for an embedded system.

REFERENCES:
2. Michael J Quinn, Parallel programming in C with MPI and OpenMP, Tata Mcgraw Hill, 2003.

VE7010 EMBEDDED NETWORKING

OBJECTIVES:
To impart knowledge on
- Serial and parallel communication protocols
- Application Development using USB and CAN bus for PIC microcontrollers
- Application development using Embedded Ethernet.
- Wireless sensor network communication protocols.


UNIT II USB AND CAN BUS:

UNIT III ETHERNET BASICS:
UNIT IV EMBEDDED ETHERNET: 9

UNIT V WIRELESS EMBEDDED NETWORKING: 9

OUTCOMES:
- Complete knowledge of wired and wireless network protocols
- Should be able to incorporate networks in embedded systems

REFERENCES:

NE7076 DIGITAL IMAGE AND VIDEO PROCESSING

OBJECTIVES:
- To provide the basic concepts of image & pattern recognition.
- To give an exposure to basic image processing and modeling techniques.
- To provide an understanding of various concepts related to video object extraction.
- To prepare students for development and implementation of algorithms

UNIT I IMAGE FUNDAMENTALS AND TRANSFORMS 9
Image Representation- Sampling and Quantization - Two dimensional DFT- Discrete cosine Transform - Walsh - Hadamard transform - Wavelet transform - Construction of Wavelets-Types of wavelets - principal component analysis.

UNIT II PROCESSING AND MODELING OF IMAGES 9
Pre-processing -Point operations – contrast stretching – Histogram - Histogram equalization - Image segmentation- pixel based, edge based, region based segmentation - Morphological image processing - Edge and texture models - Image registration - Colour Image Processing -

UNIT III SPATIAL FEATURE EXTRACTION 9
Feature selection - Localized feature extraction- Boundary Descriptors - Moments - Texture Descriptors - Co-occurrence features

UNIT IV CLASSIFIERS 9
Kernel based approaches - clustering methods - Maximum Likelihood Estimation- Bayesian approach- Pattern Classification
UNIT V  VIDEO OBJECT EXTRACTION  
Back ground subtraction – Frame difference - Static and dynamic background modeling - optical flow techniques-Handling occlusion- scale and appearance changes - Shadow removal.

TOTAL: 45 PERIODS

OUTCOMES:
- To be able to design pattern recognition systems.
- To design and implement feature extraction techniques for a given application.
- To design a suitable classifier for a given application.

REFERENCES:

VE7006  DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES  

OBJECTIVES:
- To understand the architecture and programming of fixed and floating point DSP processors.
- To understand the techniques involved in real time DSP system design and to design and implement a variety of DSP algorithms for real world applications.
- To gain the practical knowledge of real time implementation issues.
- Learn the basic forms of FIR and IIR filters, and design filters with desired frequency responses.
- Understand the fast implementation schemes of DFT.
- Learn to apply adaptive filter theory and implement it in DSP Processor.

UNIT I  INTRODUCTION TO DIGITAL SIGNAL PROCESSING SYSTEMS  
Fundamentals of DSP - Digital signal processor architectures – Software developments – Hardware issues – System considerations – Implementation considerations, Data representations, Finite word length effects, Programming issues, Real time implementation considerations.

UNIT II  FIXED AND FLOATING POINT DIGITAL SIGNAL PROCESSORS  
TMS320C55x – Architecture overview, Addressing modes, Instruction set, Programming considerations, system issues. TMS320C62x AND TMS320C64x - Architecture overview, Memory systems, External memory addressing, Instruction set, Programming considerations, system issues. TMS320C67X – Architecture overview, Instruction set, Pipeline Architecture, Programming considerations, Realtime implementations.

UNIT III  FAST FOURIER TRANSFORMS  
Introduction to DFT – FFT algorithms – Decimation-in-time, Decimation-in-frequency - Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

UNIT IV  FIR AND IIR FILTER IMPLEMENTATIONS  
FIR and IIR filters – Characteristics, Structures, FIR Filter design using Windowing and frequency sampling method, IIR Filter-Butterworth and Chebyshev Filter Design-, Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.
UNIT V  ADAPTIVE FILTER STRUCTURES AND ALGORITHMS

Wiener filter, LS filter, Filter structures, Adaptive algorithms, Properties and Applications – Fixed and floating point implementation using TMS320C64x and TMS320C67x.

TOTAL: 45 PERIODS

OUTCOMES:
- To be able to develop the program for fixed and floating point DSP processors based on the design issues.
- To be able to design and develop real time implementations on DSP algorithms.
- Ability to design IIR and FIR filters.
- To apply the fast transforms for the analysis of DSP systems.
- To be able to realize and implement a suitable structure for FIR and IIR Filters.
- To be able to design adaptive filter algorithms.

REFERENCES:
5. TMS Manual on TMS320C64XX and TMS320C67XX.